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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,993	06/23/2003	Brian J. Galloway	10030039-1	9831

7590 08/12/2004

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,993	GALLOWAY ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 are presented in the instant application according to the Applicants' filing on 06/23/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Drawings Objection

2. The drawings are objected to because of lacking "Prior Art" label in figure 7 and figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections/Minor Informalities

3. Claims 21 is objected to because of the following informalities:

Line 4, replace "ploarity" with --polarity--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant Admitted Prior Art (Fig. 1).

With respect to claim 1, Applicant Admitted Prior Art (Fig. 1) discloses a method for bridging the dead-band when a signal having a first frequency [Fref] is compared against a signal having a second frequency [Fvco], the method comprising developing from the second frequency signal a pair of phase related signals [Fi, Fq] each of the phase related signals having the same frequency but phase shifted from each other, the same frequency being controlled by the second frequency signal; and comparing [12] the first signal against each of the phase related signals to generate an error signal which quadrature rotates *(see pg 5,[0025], line 2)* when the first and second frequency signals differ in frequency from each other.

With respect to claim 2, Applicant Admitted Prior Art (Fig. 1) discloses a step of generating a control signal [ENABLE] when the quadrature rotation is outside a certain limit.

With respect to claim 3, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is controllable.

With respect to claim 4, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is different for different quadrature rotation directions.

With respect to claim 5, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, the step of generating output signals based on mismatches between the first frequency signal [Fref] and each of said generated phase-shifted signals [Fi, Fq], deriving a frequency divided signal [64] from the first frequency signal; and clocking the output signals against the frequency divided signal.

With respect to claim 6, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, the step of adjusting [62,63] the frequency divided signal to control the certain limit.

With respect to claim 7, Applicant Admitted Prior Art (Fig. 1) discloses a system for bridging the dead-band when a first signal having a first frequency [Fref] is compared against a second signal having a second frequency [Fvco], the system comprising circuitry for developing from one of said signals a pair of phase related signals [Fi, Fq] each of the phase related signals having the same frequency as the signal from which the phase related signals and developed; and comparing circuitry [12] for comparing the other of the signals against each of the phase related signals to generate an error signal which quadrature rotates *(see pg 5, [0025], line 2)* when the first and second signals differ in frequency from each other.

With respect to claim 8, Applicant Admitted Prior Art (Fig. 1) discloses the step of generating circuitry for generating a control signal when the quadrature rotation is outside a certain limit.

With respect to claim 9, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is controllable.

With respect to claim 10, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is different for different quadrature rotation directions.

With respect to claim 11, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, that the comparing circuitry comprises a) circuitry for generating output signals based on mismatches between the other [Fref] of the signals and each of the generated phase-shifted signals [Fi, Fq]; b) circuitry for deriving [64] a frequency divided signal from said other of the signals; and c) circuitry for clocking the output signals against the frequency divided signal.

With respect to claim 12, Applicant Admitted Prior Art discloses, in Fig. 6A, circuitry for adjusting [62,63] the frequency divided signal to control the certain limit.

With respect to claim 13, Applicant Admitted Prior Art discloses, in Fig. 1, a circuit for comparing two asynchronous signals, the circuit comprising a phase detector [11], a frequency detector [12] for detecting both the magnitude and polarity of any frequency difference between the signals, the frequency detector yielding control of the circuit to the phase detector when the frequency difference is within a dead-band region; and [inside [12] for generating "ENABLE" and [16]] circuitry for bridging glitches within the dead-band for a period of time to insure that the frequency difference is not outside a certain limit.

With respect to claim 14, Applicant Admitted Prior Art discloses, in Fig. 1, circuitry for developing [16] from a first one of the signals a pair of phase related signals each the phase related signal having the same frequency as first one of the signals but phase shifted 90 degrees therefrom; and circuitry for comparing [inside [12] for generating "ENABLE"] a second one of the signals against each of the phase-related signals to generate a quadrature rotating error signal when the compared signals differ in frequency from each other, wherein the speed of the quadrature rotation controls the certain limit.

With respect to claim 15, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is controllable.

With respect to claim 16, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is different for different quadrature rotation directions.

With respect to claim 17, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, that the comparing circuitry comprises a) circuitry for generating output signals based on mismatches between the other [Fref] of the signals and each of the generated phase-shifted signals [Fi, Fq]; b) circuitry for deriving [64] a frequency divided signal from said other of the signals; and c) circuitry for clocking the output signals against the frequency divided signal.

With respect to claim 18, Applicant Admitted Prior Art discloses, in Fig. 6A, circuitry for adjusting [62,63] the frequency divided signal to control the certain limit.

With respect to claim 19, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, a method for comparing two asynchronous signals, the method comprising the steps of comparing [12] the phase of said signals; comparing [12] both the magnitude and polarity of any frequency difference between the signals to yield control to the phase comparison when the frequency difference is within a dead-band region, generating quadrature signals [Fi, Fq] from one of the compared signals; comparing the other [Freq] of the signals against the quadrature signals to yield a signal which has a speed of rotation having a relationship to any mismatch between the signals, and bridging glitches within the dead-band for a period of time to insure that the compared signals are not outside a certain limit, the bridging a function of the speed of the phase rotation.

With respect to claim 20, Applicant Admitted Prior Art (Fig. 1) discloses that the certain limit is controllable.

With respect to claim 21, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, a VCO circuit having a VCO output voltage and a reference voltage, the circuit comprising a phase detector [11]; a frequency detector [12] for detecting both the magnitude and polarity of any frequency difference between the reference signal and the VCO output voltage, the frequency detector yielding control of the circuit to the phase detector when the frequency difference is within a dead-band region; and circuitry for bridging glitches [inside [12] for generating "ENABLE" and [16]] within the dead-band for a period of time to insure that the compared signals are not outside a certain limit.

With respect to claim 22, Applicant Admitted Prior Art discloses, in Figs. 1 and 6A, circuitry [divider 16] for developing from the VCO output voltage a pair of phase related signals each the phase related signal having the same frequency as the VCO output voltage but phase shifted go degrees therefrom; and circuitry [Part of 12] for comparing the reference signal against each of the developed signals to generate a quadrature rotating an error signal when the reference signal and the VCO output voltage are out of frequency with each other, wherein the speed of the quadrature rotation controls the certain limit.

Citation of Relevant Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Dalmia (U.S. Patent No. 6,310,521) discloses a reference-free clock generation and data recovery PLL.

Prior art Larsson (U.S. Patent No. 6,392,495) discloses a frequency detector circuits and systems.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER